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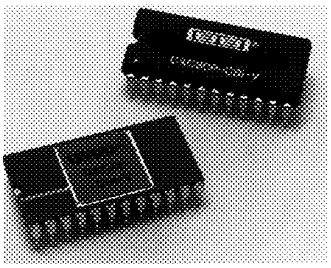


DAC80
DAC80P

Monolithic 12-Bit DIGITAL-TO-ANALOG CONVERTERS

FEATURES

- **INDUSTRY STANDARD PINOUT**
- **FULL ±10V SWING WITH V_{CC} = ±12VDC**
- **DIGITAL INPUTS ARE TTL- AND CMOS-COMPATIBLE**
- **GUARANTEED SPECIFICATIONS WITH ±12V AND ±15V SUPPLIES**
- **±1/2LSB MAXIMUM NONLINEARITY: 0°C to +70°C**
- **SETTLING TIME: 4µs max to ±0.01% of Full Scale**
- **GUARANTEED MONOTONICITY: 0°C to +70°C**
- **TWO PACKAGE OPTIONS: Hermetic side-brazed ceramic and low-cost molded plastic**

DESCRIPTION

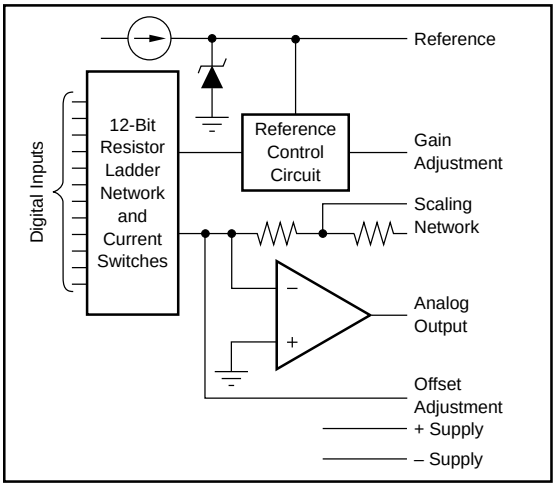
This monolithic digital-to-analog converter is pin-for-pin equivalent to the industry standard DAC80 first introduced by Burr-Brown. Its single-chip design includes the output amplifier and provides a highly stable reference capable of supplying up to 2.5mA to an external load without degradation of D/A performance.

This converter uses proven circuit techniques to provide accurate and reliable performance over temperature and power supply variations. The use of a buried zener diode as the basis for the internal reference contributes to the high stability and low noise of the device. Advanced methods of laser trimming result in precision output current and output amplifier feedback resistors, as well as low integral and differential linearity errors. Innovative circuit design enables the DAC80 to operate at supply voltages as low as ±11.4V with no loss in performance or accuracy over any range of output voltage. The lower power dissipation of this 118-mil by 121-mil chip results in higher reliability and greater long term stability.

Burr-Brown has further enhanced the reliability of the monolithic DAC80 by offering a hermetic, side-brazed, ceramic package. In addition, ease of use has been enhanced by eliminating the need for a +5V logic power supply.

For applications requiring both reliability and low cost, the DAC80P in a molded plastic package offers the same electrical performance over temperature as the ceramic model. The DAC80P is available with voltage output only.

For designs that require a wider temperature range, see Burr-Brown models DAC85H and DAC87H.



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SBAS148

SPECIFICATIONS

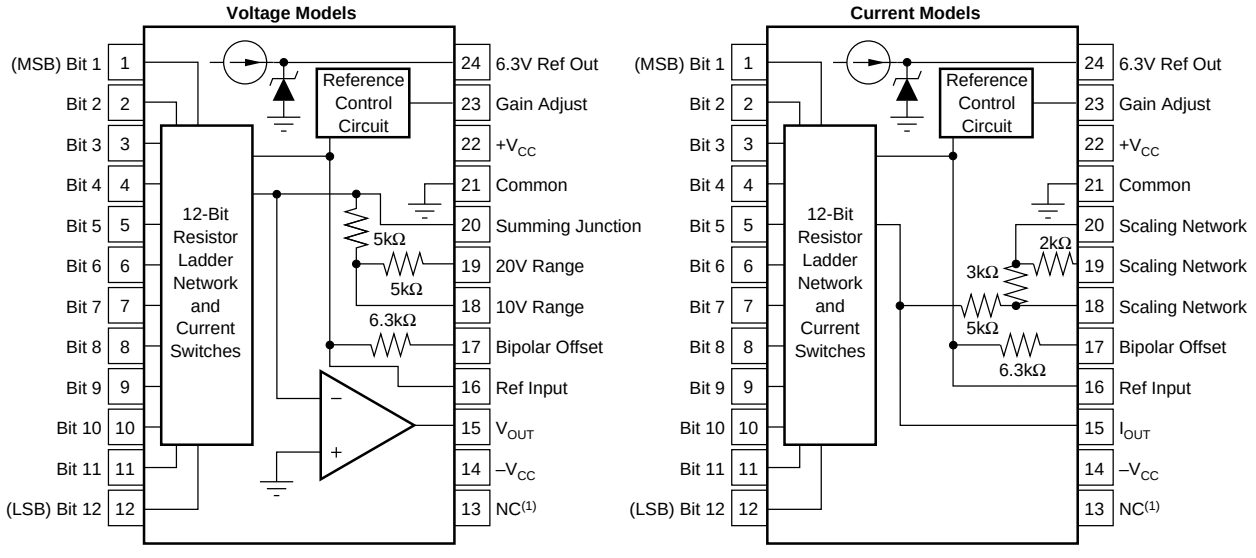
ELECTRICAL

Typical at +25°C and $\pm V_{CC}$ = 12V or 15V unless otherwise noted.

PARAMETER	DAC80 MIN	DAC80 TYP	DAC80 MAX	UNITS
DIGITAL INPUT				
Resolution			12	Bits
Logic Levels (0°C to +70°C)[1]:				
V_{IH} (Logic "1")	+2		+16.5	VDC
V_{IL} (Logic "0")	0		+0.8	VDC
I_{IH} (V_{IN} = +2.4V)			+20	µA
I_{IL} (V_{IN} = +0.4V)			–180	µA
ACCURACY (at +25°C)				
Linearity Error		±1/4	±1/2	LSB
Differential Linearity Error		±1/2	±3/4	LSB
Gain Error[2]		±0.1	±0.3	%
Offset Error[2]		±0.05	±0.15	% of FSR[3]
DRIFT (0°C to +70°C)[4]				
Total Bipolar Drift (includes gain, offset, and linearity drifts)		±10	±25	ppm of FSR/°C
Total Error Over 0°C to +70°C[5]				
Unipolar		±0.06	±0.15	% of FSR
Bipolar		±0.06	±0.12	% of FSR
Gain: Including Internal Reference		±10	±30	ppm/°C
Excluding Internal Reference		±5	±10	ppm/°C
Unipolar Offset		±1	±3	ppm of FSR/°C
Bipolar Offset		±7	±15	ppm of FSR/°C
Differential Linearity 0°C to +70°C		±1/2	±3/4	LSB
Linearity Error 0°C to +70°C		±1/4	±1/2	LSB
Monotonicity Guaranteed	0		+70	°C
CONVERSION SPEED, V_{OUT} Models				
Settling Time to ±0.01% of FSR				
For FSR Change (2kΩ || 500pF Load)				
with 10kΩ Feedback		3	4	µs
with 5kΩ Feedback		2	3	µs
For 1LSB Change		1		µs
Slew Rate	10			V/µs
CONVERSION SPEED, I_{OUT} Models				
Settling Time to ±0.01% of FSR				
For FSR change: 10Ω to 100Ω Load		300		ns
1kΩ Load		1		µs
ANALOG OUTPUT, V_{OUT} Models				
Ranges		±2.5, ±5, ±10, +5, +10		V
Output Current[6]	±5			mA
Output Impedance (DC)		0.05		Ω
Short Circuit to Common, Duration[7]		Indefinite		
ANALOG OUTPUT, I_{OUT} Models				
Ranges: Bipolar	±0.96	±1.0	±1.04	mA
Unipolar	–1.96	–2.0	–2.04	mA
Output Impendance: Bipolar	2.6	3.2	3.7	kΩ
Unipolar	4.6	6.6	8.6	kΩ
Compliance	–2.5		+2.5	V
REFERENCE VOLTAGE OUTPUT	+6.23	+6.30	+6.37	V
External Current (constant load)			2.5	mA
Drift vs Temperature		±10	±20	ppm/°C
Output Impedance		1		Ω
POWER SUPPLY SENSITIVITY				
V_{CC} = ±12VDC or ±15VDC		±0.002	±0.006	% FSR/ % V_{CC}
POWER SUPPLY REQUIREMENTS				
$\pm V_{CC}$	±11.4		±16.5	VDC
Supply Drain (no load): $+V_{CC}$		8	12	mA
$-V_{CC}$		15	20	mA
Power Dissipation (V_{CC} = ±15VDC)		345	480	mW
TEMPERATURE RANGE				
Specification	0		+70	°C
Operating	–25		+85	°C
Storage: Plastic DIP	–60		+100	°C
Ceramic DIP	–65		+150	°C

NOTES: (1) Refer to "Logic Input Compatibility" section. (2) Adjustable to zero with external trim potentiometer. (3) FSR means full scale range and is 20V for ±10V range, 10V for ±5V range for V_{OUT} models; 2mA for I_{OUT} models. (4) To maintain drift spec, internal feedback resistors must be used. (5) Includes the effects of gain, offset and linearity drift. Gain and offset errors externally adjusted to zero at +25°C. (6) For $\pm V_{CC}$ less than ±12VDC, limit output current load to ±2.5mA to maintain ±10V full scale output voltage swing. For output range of ±5V or less, the output current is ±5mA over entire $\pm V_{CC}$ range. (7) Short circuit current is 40mA, max.

FUNCTIONAL DIAGRAM AND PIN ASSIGNMENTS



NOTE: (1) Logic supply applied to this pin has no effect.

ABSOLUTE MAXIMUM RATINGS

$+V_{CC}$ to Common	0V to +18V
$-V_{CC}$ to Common	0V to –18
Digital Data Inputs to Common	–1V to +18V
Reference Output to Common	$\pm V_{CC}$
Reference Input to Common	$\pm V_{CC}$
Bipolar Offset to Common	$\pm V_{CC}$
10V Range R to Common	$\pm V_{CC}$
20V Range R to Common	$\pm V_{CC}$
External Voltage to DAC Output	–5V to +5V
Lead Temperature (soldering, 10s)	+300°C
Max Junction Temperature	165°C
Thermal Resistance, θ_{JA}: Plastic DIP	100°C/W
Ceramic DIP	65°C/W

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods may affect device reliability.

ORDERING INFORMATION

MODEL	PACKAGE	OUTPUT
DAC80-CBI-I	Ceramic DIP	Current
DAC80Z-CBI-I	Ceramic DIP	Current
DAC80-CBI-V	Ceramic DIP	Voltage
DAC80Z-CBI-V	Ceramic DIP	Voltage
DAC80P-CBI-V	Plastic DIP	Voltage
BURN-IN SCREENING OPTION		
MODEL	**PACKAGE**	**BURN-IN TEMP. (160h)(1)**
DAC80-CBI-V-BI	Ceramic DIP	+125°C
DAC80P-CBI-V-BI	Plastic DIP	+125°C

NOTE: (1) Or equivalent combination. See text.

PACKAGE INFORMATION

MODEL	PACKAGE	PACKAGE DRAWING NUMBER(1)
DAC80P	24-Pin Plastic DIP	167
DAC80	24-Pin Ceramic DIP	125

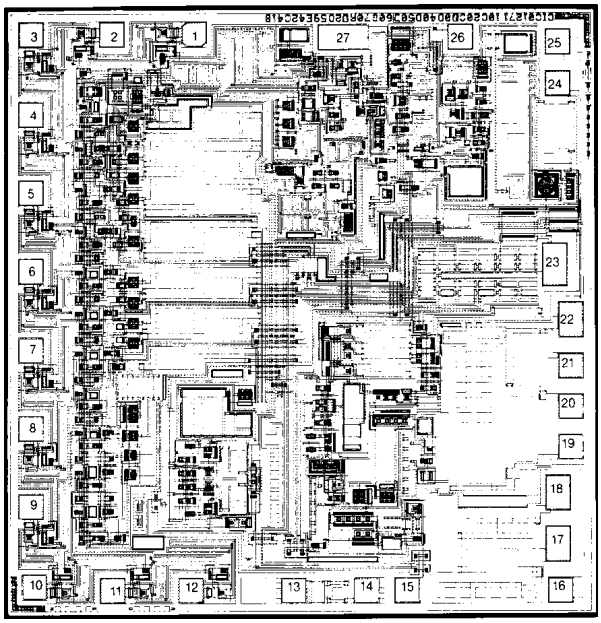
NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix D of Burr-Brown IC Data Book.

BURN-IN SCREENING

Burn-in screening is an option available for the models indicated in the Ordering Information table. Burn-in duration is 160 hours at the maximum specified grade operating temperature (or equivalent combination of time and temperature).

All units are tested after burn-in to ensure that grade specifications are met. To order burn-in, add "–BI" to the base model number.

DICE INFORMATION



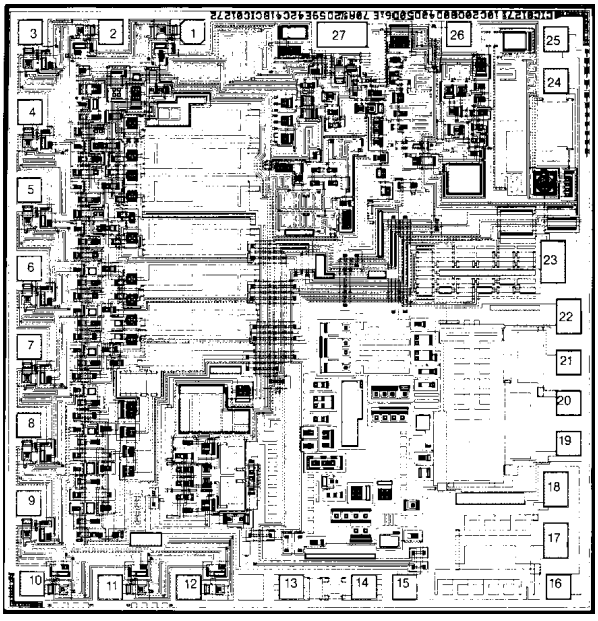
DAC80KD-V DIE TOPOGRAPHY

PAD	FUNCTION	PAD	FUNCTION
1	Bit 1 (MSB)	15	$-V_{CC}$
2	Bit 2	16	V_{OUT}
3	Bit 3	17	Ref In
4	Bit 4	18	Bipolar Offset
5	Bit 5	19	Scale 10V FSR
6	Bit 6	20	Scale 20V FSR
7	Bit 7	21	NC
8	Bit 8	22	Sum Junct
9	Bit 9	23	COM
10	Bit 10	24	COM
11	Bit 11	25	$+V_{CC}$
12	Bit 12 (LSB)	26	Gain Adjust
13	NC	27	6.3V Ref Out
14	NC		

Substrate Bias: Isolated. NC: No Connection

MECHANICAL INFORMATION

	MILS (0.001")	MILLIMETERS
Die Size	118 x 121 ± 5	3.0 x 3.07 ± 0.13
Die Thickness	20 ± 3	0.51 ± 0.08
Min. Pad Size	4 x 4	0.10 x 0.10
Metalization		Aluminum



DAC80KD-I DIE TOPOGRAPHY

PAD	FUNCTION	PAD	FUNCTION
1	Bit 1 (MSB)	15	$-V_{CC}$
2	Bit 2	16	I_{OUT}
3	Bit 3	17	Ref In
4	Bit 4	18	Bipolar Offset
5	Bit 5	19	Scale 10V FSR
6	Bit 6	20	Scale 20V FSR
7	Bit 7	21	Scale
8	Bit 8	22	NC
9	Bit 9	23	COM
10	Bit 10	24	COM
11	Bit 11	25	$+V_{CC}$
12	Bit 12 (LSB)	26	Gain Adjust
13	NC	27	6.3V Ref Out
14	NC		

Substrate Bias: Isolated. NC: No Connection

MECHANICAL INFORMATION

	MILS (0.001")	MILLIMETERS
Die Size	118 x 121 ± 5	3.0 x 3.07 ± 0.13
Die Thickness	20 ± 3	0.51 ± 0.08
Min. Pad Size	4 x 4	0.10 x 0.10
Metalization		Aluminum

DISCUSSION OF SPECIFICATIONS

DIGITAL INPUT CODES

The DAC80 accepts complementary binary digital input codes. The CBI model may be connected by the user for any one of three complementary codes: CSB, COB, or CTC (see Table I).

DIGITAL INPUT	ANALOG OUTPUT		
MSB ↓ LSB ↓	CSB Complementary Straight Binary	COB Complementary Offset Binary	CTC[1] Complementary Two's Complement
000000000000	+Full Scale	+Full Scale	–1LSB
011111111111	+1/2 Full Scale	Zero	–Full Scale
100000000000	1/2 Full Scale –1LSB	–1LSB	–Full Scale
111111111111	Zero	–Full Scale	Zero
NOTE: (1) Invert the MSB of the COB code with an external inverter to obtain CTC code.			

TABLE I. Digital Input Codes.

ACCURACY

Linearity of a D/A converter is the true measure of its performance. The linearity error of the DAC80 is specified over its entire temperature range. This means that the analog output will not vary by more than ±1/2LSB, maximum, from an ideal straight line drawn between the end points (inputs all "1"s and all "0"s) over the specified temperature range of 0°C to +70°C.

Differential linearity error of a D/A converter is the deviation from an ideal 1LSB voltage change from one adjacent output state to the next. A differential linearity error specification of ±1/2LSB means that the output voltage step sizes can range from 1/2LSB to 3/2LSB when the input changes from one adjacent input state to the next.

Monotonicity over a 0°C to +70°C range is guaranteed in the DAC80 to insure that the analog output will increase or remain the same for increasing input digital codes.

DRIFT

Gain Drift is a measure of the change in the full scale range output over temperature expressed in parts per million per °C (ppm/°C). Gain drift is established by: 1) testing the end point differences for each DAC80 model at 0°C, +25°C, and +70°C; 2) calculating the gain error with respect to the 25°C value, and; 3) dividing by the temperature change. This figure is expressed in ppm/°C and is given in the electrical specifications both with and without internal reference.

Offset Drift is a measure of the actual change in output with all "1"s on the input over the specified temperature range. The offset is measured at 0°C, +25°C, and 70°C. The maximum change in Offset is referenced to the Offset at 25°C and is divided by the temperature range. This drift is expressed in parts per million of full scale range per °C (ppm of FSR/°C).

SETTLING TIME

Settling time for each DAC80 model is the total time (including slew time) required for the output to settle within an error band around its final value after a change in input (see Figure 1).

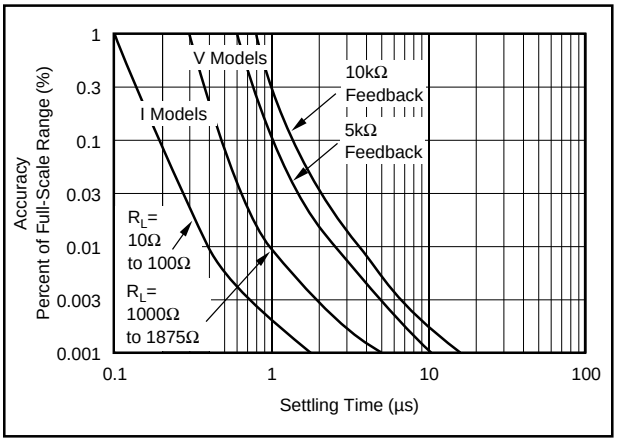


FIGURE 1. Full Scale Range Settling Time vs Accuracy.

Voltage Output Models

Three settling times are specified to ±0.01% of full scale range (FSR); two for maximum full scale range changes of 20V, 10V and one for a 1LSB change. The 1LSB change is measured at the major carry (0111...11 to 1000...00), the point at which the worst case settling time occurs.

Current Output Models

Two settling times are specified to ±0.01% of FSR. Each is given for current models connected with two different resistive loads: 10Ω to 100Ω and 1000Ω to 1875Ω. Internal resistors are provided for connecting nominal load resistances of approximately 1000Ω to 1800Ω for output voltage range of ±1V and 0 to –2V (see Figures 11 and 12).

COMPLIANCE

Compliance voltage is the maximum voltage swing allowed on the current output node in order to maintain specified accuracy. The maximum compliance voltage of all current output models is ±2.5V. Maximum safe voltage range of ±1V and 0 to –2V (see Figures 11 and 12).

POWER SUPPLY SENSITIVITY

Power supply sensitivity is a measure of the effect of a power supply change on the D/A converter output. It is defined as a percent of FSR per percent of change in either the positive or negative supplies about the nominal power supply voltages (see Figure 2).

REFERENCE SUPPLY

All DAC80 models are supplied with an internal 6.3V reference voltage supply. This voltage (pin 24) has a tolerance of ±1% and must be connected to the Reference Input

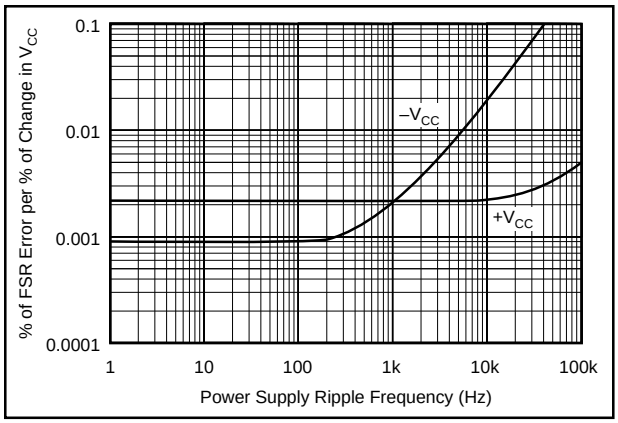


FIGURE 2. Power Supply Rejection vs Power Supply Ripple.

(pin 16) for specified operation. This reference may be used externally also, but external current drain is limited to 2.5mA.

If a varying load is to be driven, an external buffer amplifier is recommended to drive the load in order to isolate bipolar offset from load variations. Gain and bipolar offset adjustments should be made under constant load conditions.

LOGIC INPUT COMPATIBILITY

DAC80 digital inputs are TTL, LSTTL and 4000B, 54/74HC CMOS compatible. The input switching threshold remains at the TTL threshold over the entire supply range.

Logic "0" input current over temperature is low enough to permit driving DAC80 directly from outputs of 4000B and 54/74C CMOS devices.

OPERATING INSTRUCTIONS

POWER SUPPLY CONNECTIONS

Connect power supply voltages as shown in Figure 3. For optimum performance and noise rejection, power supply decoupling capacitors should be added as shown. These capacitors (1µF tantalum) should be located close to the DAC80.

±12V OPERATION

All DAC80 models can operate over the entire power supply range of ±11.4V to ±16.5V. Even with supply levels dropping to ±11.4V, the DAC80 can swing a full ±10V range, provided the load current is limited to ±2.5mA. With power supplies greater than ±12V, the DAC80 output can be loaded up to ±5mA. For output swing of ±5V or less, the output current is ±5mA, minimum, over the entire V_{CC} range.

No bleed resistor is needed from $+V_{CC}$ to pin 24, as was needed with prior hybrid Z versions of DAC80. Existing ±12V applications that are being converted to the monolithic DAC80 must omit the resistor to pin 24 to insure proper operation.

EXTERNAL OFFSET AND GAIN ADJUSTMENT

Offset and gain may be trimmed by installing external Offset and Gain potentiometers. Connect these potentiometers as shown in Figure 3 and adjust as described below. TCR of the potentiometers should be 100ppm/°C or less. The 3.9MΩ and 10MΩ resistors (20% carbon or better) should be located close to the DAC80 to prevent noise pickup. If it is not convenient to use these high value resistors, an equivalent "T" network, as shown in Figure 4, may be substituted.

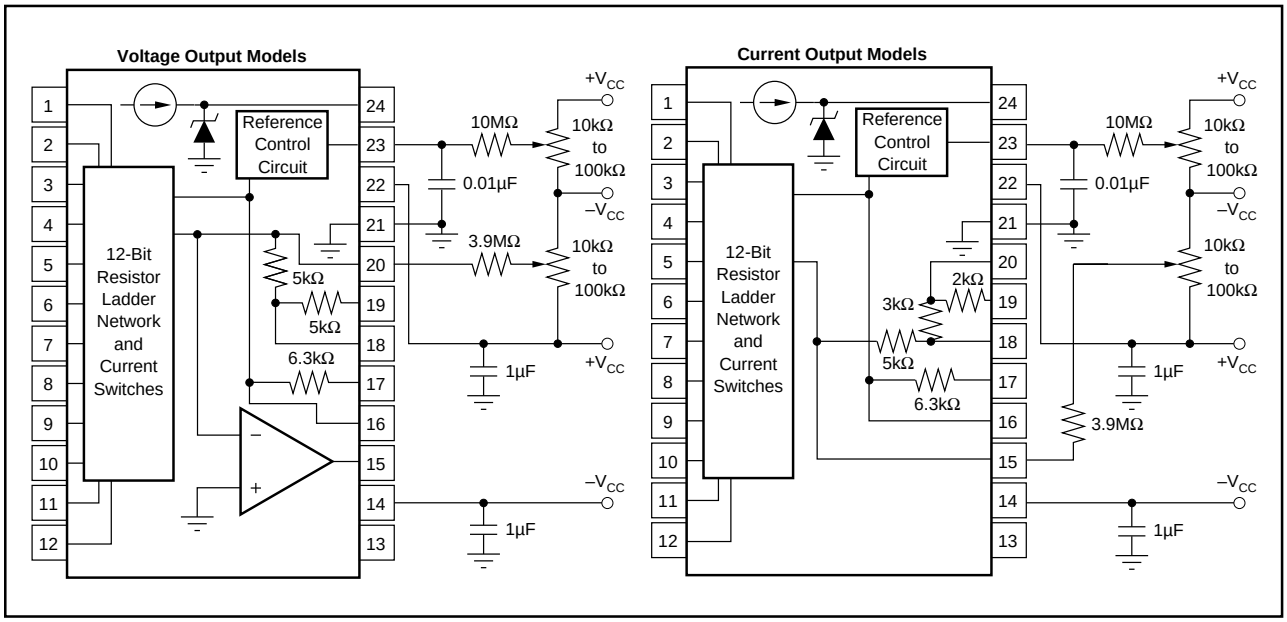


FIGURE 3. Power Supply and External Adjustment Connection Diagrams.

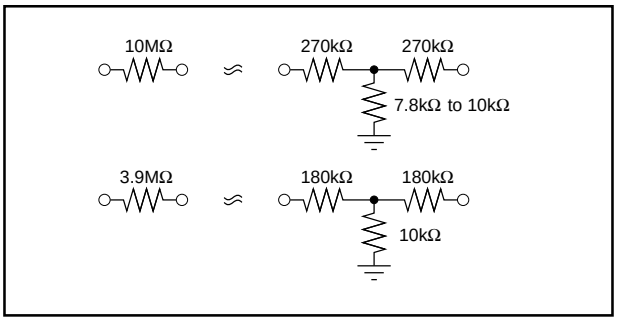


FIGURE 4. Equivalent Resistances.

Existing applications that are converting to the monolithic DAC80 must change the gain trim resistor on pin 23 from 33MΩ to 10MΩ to insure sufficient adjustment range. Pin 23 is a high impedance point and a 0.001µ1F to 0.01µF ceramic capacitor should be connected from this pin to Common (pin 21) to prevent noise pickup. Refer to Figure 5 for relationship of Offset and Gain adjustments to unipolar and bipolar D/A operation.

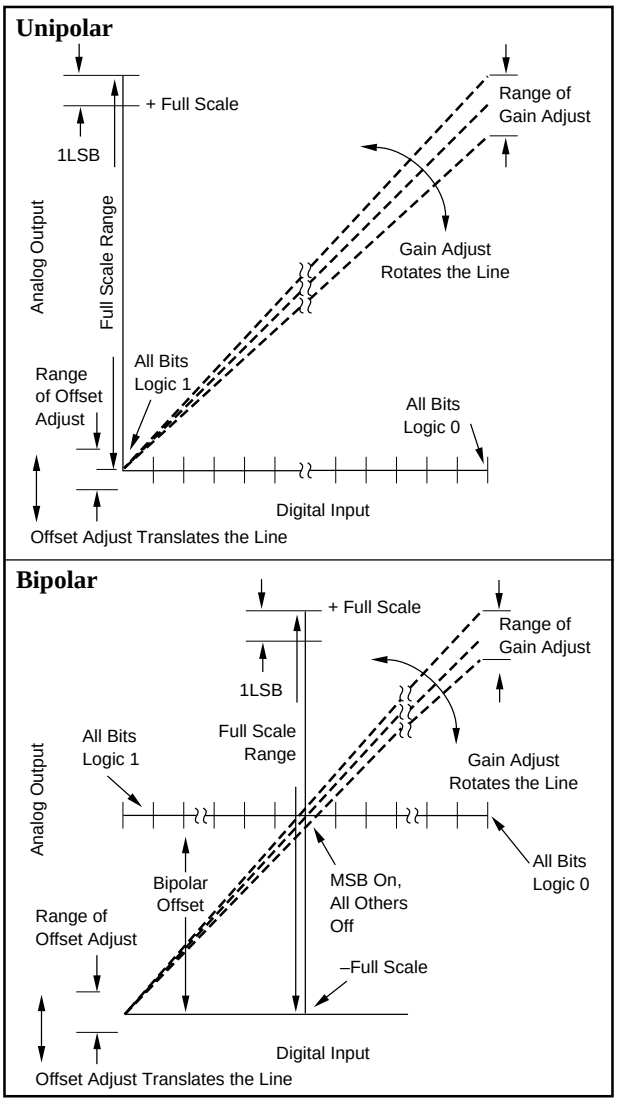


FIGURE 5. Relationship of Offset and Gain Adjustments for a Unipolar and Bipolar D/A Converter.

Offset Adjustment

For unipolar (CSB) configurations, apply the digital input code that should produce zero potential output and adjust the Offset potentiometer for zero output.

For bipolar (COB, CTC) configurations, apply the digital input code that should produce the maximum negative output. Example: If the Full Scale Range is connected for 20V, the maximum negative output voltage is –10V. See Table II for corresponding codes.

Gain Adjustment

For either unipolar or bipolar configurations, apply the digital input that should give the maximum positive output. Adjust the Gain potentiometer for this positive full scale output. See Table II for positive full scale voltages and currents.

	ANALOG OUTPUT			
DIGITAL INPUT	VOLTAGE(1)		CURRENT	
MSB ↓ LSB ↓	0 to +10V	±10V	0 to –2mA	±1mA
000000000000	+9.9976V	+9.9951V	–1.9995mA	–0.9995mA
011111111111	+5.0000V	0.0000V	–1.0000mA	0.0000mA
100000000000	+4.9976V	–0.0049V	–0.9995mA	+0.0005mA
111111111111	0.0000V	–10.0000V	0.0000mA	+1.000mA
One LSB	2.44mV	4.88mV	0.488µA	0.488µA

NOTE: (1) To obtain values for other binary ranges:
0 to +5V range divide 0 to +10V range values by 2.
±5V range: divide ±10V range values by 2.
±2.5V range: divide ±10V range values by 4.

TABLE II. Digital Input/Analog Output.

VOLTAGE OUTPUT MODELS

Output Range Connections

Internal scaling resistors provided in the DAC80 may be connected to produce bipolar output voltage ranges of ±10V, ±5V, or ±2.5V; or unipolar output voltage ranges of 0 to +5V or 0 to +10V. See Figure 6.

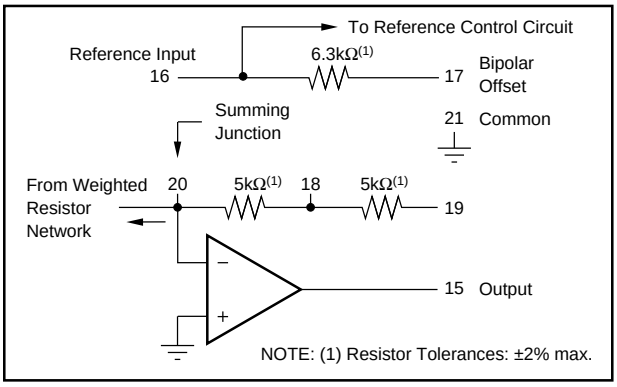


FIGURE 6. Output Amplifier Voltage Range Scaling Circuit.

Gain and offset drift are minimized because of the thermal tracking of the scaling resistors with other internal device components. Connections for various output voltage ranges are shown in Table III. Settling time for a full-scale range change is specified as 4µs for the 20V range and 3µs for the 10V range.

Output Range	Digital Input Codes	Connect Pin 15 to	Connect Pin 17 to	Connect Pin 19 to	Connect Pin 16 to
±10	COB or CTC	19	20	15	24
±5	COB or CTC	18	20	NC	24
±2.5V	COB or CTC	18	20	20	24
0 to +10V	CSB	18	21	NC	24
0 to +5V	CSB	18	21	20	24

TABLE III. Output Voltage Range Connections for Voltage Models.

CURRENT OUTPUT MODELS

The resistive scaling network and equivalent output circuit of the current model differ from the voltage model and are shown in Figures 7 and 8.

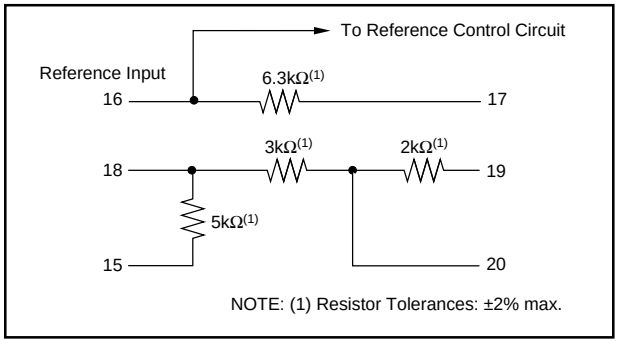


FIGURE 7. Internal Scaling Resistors.

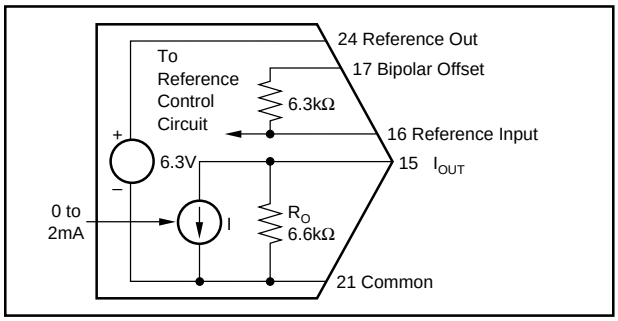


FIGURE 8. Current Output Model Equivalent Output Circuit.

Internal scaling resistors (Figure 7) are provided to scale an external op amp or to configure load resistors for a voltage output. These connections are described in the following sections.

If the internal resistors are not used for voltage scaling, external R_L (or R_F) resistors should have a TCR of ±25ppm/°C or less to minimize drift. This will typically add ±50ppm/°C plus the TCR of R_L (or R_F) to the total drift.

Driving An External Op Amp

The current output model DAC80 will drive the summing junction of an op amp used as a current-to-voltage converter to produce an output voltage. See Figure 9.

$$V_{OUT} = I_{OUT} \times R_F$$

where I_{OUT} is the DAC80 output current and R_F is the feedback resistor. Using the internal feedback resistors of

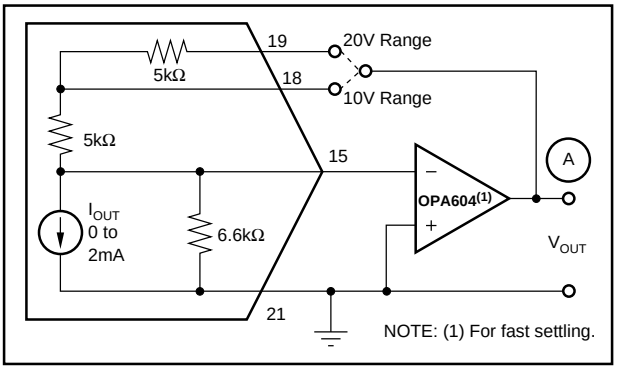


FIGURE 9. External Op-Amp—Using Internal Feedback Resistors.

the current output model DAC80 provides output voltage ranges the same as the voltage model DAC80. To obtain the desired output voltage range when connecting an external op amp, refer to Table IV.

Output Range	Digital Input Codes	Connect Ⓐ to	Connect Pin 17 to	Connect Pin 19 to	Connect Pin 16 to
±10V	COB or CTC	19	15	Ⓐ	24
±5V	COB or CTC	18	15	NC	24
±2.5V	COB or CTC	18	15	15	24
0 to +10V	CSB	18	21	NC	24
0 to +5V	CSB	18	21	15	24

TABLE IV. Voltage Range of Current Output.

Output Larger Than 20V Range

For output voltage ranges larger than ±10V, a high voltage op amp may be employed with an external feedback resistor. Use I_{OUT} value of ±1mA for bipolar voltage ranges and –2mA for unipolar voltage ranges. See Figure 10. Use protection diodes when a high voltage op amp is used.

The feedback resistor, R_F, should have a temperature coefficient as low as possible. Using an external feedback resistor, overall drift of the circuit increases due to the lack of temperature tracking between R_F and the internal scaling resistor network. This will typically add 50ppm/°C plus R_F drift to total drift.

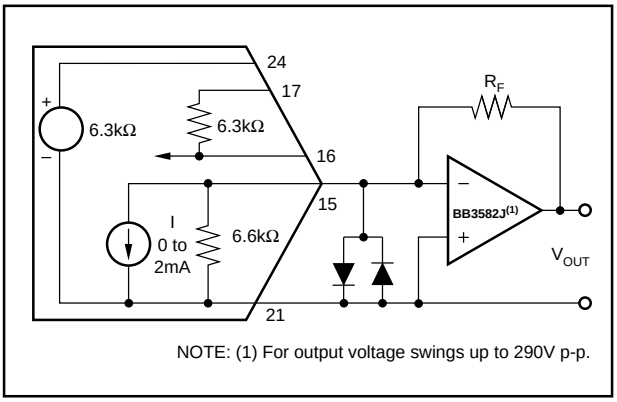


FIGURE 10. External Op-Amp—Using External Feedback Resistors.

Driving a Resistive Load Unipolar

A load resistance, $R_L = R_{LI} + R_{LS}$, connected as shown in Figure 11 will generate a voltage range, V_{OUT}, determined by:

$$V_{OUT} = -2mA\ [(R_L \times R_O) \div (R_L + R_O)]$$

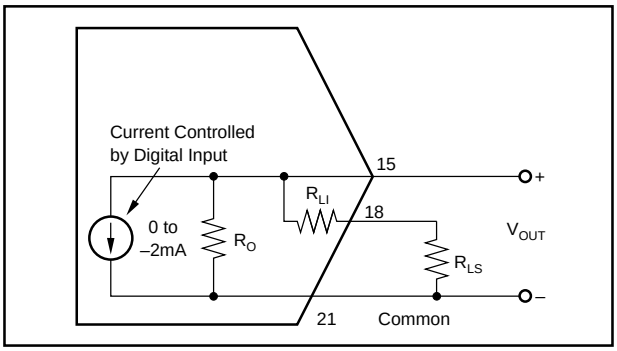


FIGURE 11. Current Output Model Equivalent Circuit Connected for Unipolar Voltage Output with Resistive Load.

The unipolar output impedance R_O equals 6.6kΩ (typ) and R_{LI} is the internal load resistance of 968Ω (derived by connecting pin 15 to 20 and pin 18 to 19). By choosing R_{LS} = 210Ω, R_L = 1178Ω. R_L in parallel with R_O yields 1kΩ total load. This gives an output range of 0 to –2V. Since R_O is not exact, initial trimming per Figure 3 may be necessary; also R_{LS} may be trimmed.

Driving a Resistive Load Bipolar

The equivalent output circuit for a bipolar output voltage range is shown in Figure 12, $R_L = R_{LI} + R_{LS}$. V_{OUT} is determined by:

$$V_{OUT} = \pm 1mA\ [(R_O \times R_L) \div (R_O + R_L)]$$

By connecting pin 17 to 15, the output current becomes bipolar (±1mA) and the output impedance R_O becomes 3.2kΩ (6.6kΩ in parallel with 6.3kΩ). R_{LI} is 1200Ω (derived by connecting pin 15 to 18 and pin 18 to 19). By choosing R_{LS} = 225Ω, R_L = 1455Ω. R_L in parallel with R_O yields 1kΩ total load. This gives an output range of ±1V. As indicated above, trimming may be necessary.

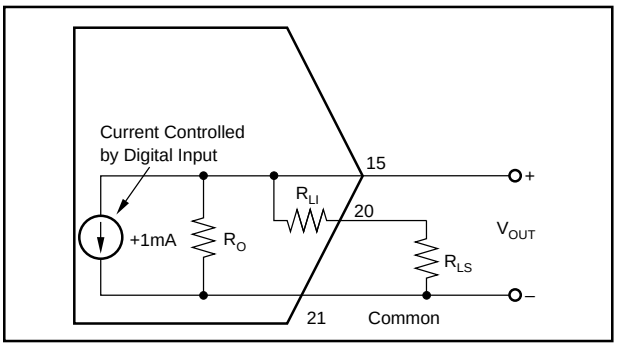


FIGURE 12. Current Output Model Connected for Bipolar Output Voltage with Resistive Load.

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Orderable Device	Status [1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [2]	Lead/Ball Finish	MSL Peak Temp [3]
DAC80-CBI-I	OBSOLETE	CDIP SB	JDM	24		TBD	Call TI	Call TI
DAC80-CBI-V	OBSOLETE	CDIP SB	JDM	24		TBD	Call TI	Call TI
DAC80KD-I	OBSOLETE	DIESALE	Y	0		TBD	Call TI	Call TI
DAC80KD-V	OBSOLETE	DIESALE	Y	0		TBD	Call TI	Call TI
DAC80P-CBI-V	OBSOLETE	PDIP	NTA	24		TBD	Call TI	Call TI
DAC80P-CBI-V-BI	OBSOLETE	PDIP	NTA	24		TBD	Call TI	Call TI
DAC80Z-CBI-V	OBSOLETE	CDIP SB	JD	24		TBD	Call TI	Call TI

[1] The marketing status values are defined as follows:
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PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
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[3] MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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